IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) An apparatus comprising:

an input transistor and a second transistor coupled as a Darlington pair; and

a bias circuit to increase a collector-to-emitter bias current in the input transistor, wherein the bias circuit comprises an operational amplifier coupled to maintain a substantially constant base voltage on the second transistor.

2. (Canceled)

3. (Canceled)

4. (Previously Presented) An apparatus comprising:

an input transistor and a second transistor coupled as a Darlington pair;

a bias circuit to increase a collector-to-emitter bias current in the input transistor; and

a cascode transistor coupled between an upper power supply node and collectors of the input and second transistors.

5. (Original) The apparatus of claim 4 further comprising a second bias circuit to bias the cascode transistor.

6. (Previously Presented) The apparatus of claim 5 further comprising a third bias circuit to apply a bias voltage to a base of the input transistor.

7. (Original) The apparatus of claim 6 wherein the input transistor comprises a heterojunction bipolar transistor.

8. (Original) The apparatus of claim 6 wherein the input transistor comprises an Indium Phospate transistor.

9. (Canceled)

10. (Original) The apparatus of claim 1 further comprising an inductor coupled to a collector of the second transistor.

11. (Original) The apparatus of claim 1 further comprising an inductor coupled to an emitter of the second transistor.

12. (Previously Presented) An apparatus comprising:

an amplifier including an input transistor and a second transistor coupled as a Darlington pair;

a controllable bias circuit coupled to an emitter of the input transistor, wherein the controllable bias circuit comprises an operational amplifier coupled to maintain a substantially constant emitter voltage on the input transistor; and

a control circuit to influence operation of the controllable bias circuit.

13. (Original) The apparatus of claim 12 further comprising a second controllable bias circuit coupled to a base of the input transistor.

14. (Canceled)

15. (Previously Presented) The apparatus of claim 12 further comprising a low pass filter between an output of the operational amplifier and the emitter of the input transistor.

16. (Original) The apparatus of claim 12 wherein the control circuit includes a digital-to-analog converter.

17. (Original) The apparatus of claim 12 wherein the control circuit includes a processor.

18. (Currently Amended) An apparatus comprising:

an amplifier including an input transistor and a second transistor coupled as a Darlington pair;

a controllable bias circuit coupled to an emitter of the input transistor;

a control circuit to influence operation of the controllable bias circuit to increase a collector-to-emitter bias current in the input transistor; and

a cascode transistor coupled between an upper power supply node and a collector of the input transistor.

19. (Original) The apparatus of claim 18 further comprising a controllable bias circuit coupled to a control node of the cascode transistor.

20. (Currently Amended) ~~The apparatus of claim 19~~ An apparatus comprising:

an amplifier including an input transistor and a second transistor coupled as a Darlington pair;

a controllable bias circuit coupled to an emitter of the input transistor;

a control circuit to influence operation of the controllable bias circuit to increase a collector-to-emitter bias current in the input transistor;

a cascode transistor coupled between an upper power supply node and a collector of the input transistor; and

a controllable bias circuit coupled to a control node of the cascode transistor, wherein the control circuit is coupled to influence operation of the controllable bias circuit for the cascode transistor.

21. (Currently Amended) ~~The apparatus of claim 19 further comprising~~ An apparatus comprising:

an amplifier including an input transistor and a second transistor coupled as a Darlington pair;

a controllable bias circuit coupled to an emitter of the input transistor;

a control circuit to influence operation of the controllable bias circuit to increase a collector-to-emitter bias current in the input transistor;

a cascode transistor coupled between an upper power supply node and a collector of the input transistor;

a controllable bias circuit coupled to a control node of the cascode transistor, and

an automatic gain control circuit coupled between an output of the amplifier and the controllable bias circuit for the cascode transistor.

22. (Previously Presented) An electronic system comprising:

an antenna;

an amplifier coupled to the antenna, the amplifier including an input transistor and a second transistor coupled as a Darlington pair;

a controllable bias circuit coupled to an emitter of the input transistor, wherein the controllable bias circuit comprises an operational amplifier coupled to maintain a substantially constant emitter voltage on the input transistor; and

a control circuit to influence operation of the controllable bias circuit.

23. (Original) The electronic system of claim 22 further comprising a second controllable bias circuit coupled to a base of the input transistor.

24. (Canceled)

25. (Original) The electronic system of claim 22 wherein the control circuit comprises a processor.

26. (Previously Presented) A method comprising:

increasing a bias current in an input transistor of a Darlington pair by providing a current path from, and a voltage path to, an emitter of the input transistor; and

modifying a bias voltage on a cascode transistor coupled between an upper power supply node and the Darlington pair.

27. (Original) The method of claim 26 further comprising:

applying a reference signal to a base of the input transistor; and

measuring an output voltage of the Darlington pair.

28. (Original) The method of claim 27 further comprising modifying a bias voltage applied to the base of the input transistor.

29. (Original) The method of claim 27 wherein increasing a bias current comprises changing a bias voltage on a voltage controlled current source.

30. (Canceled)

31. (New) The apparatus of claim 20 wherein the input transistor comprises a heterojunction bipolar transistor.

32. (New) The apparatus of claim 20 wherein the input transistor comprises an Indium Phospate transistor.

33. (New) The apparatus of claim 21 wherein the input transistor comprises a heterojunction bipolar transistor.

34. (New) The apparatus of claim 21 wherein the input transistor comprises an Indium Phospate transistor.